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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,881	04/06/2006	Martinus Jacobus Coenen	NL03 1229 US	1731
65913	7590	02/07/2008		
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER CLARK, JASMINE JHIHAN B	
			ART UNIT 2815	PAPER NUMBER
			NOTIFICATION DATE 02/07/2008	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/574,881	<b>Applicant(s)</b> COENEN, MARTINUS JACOBUS	
	<b>Examiner</b> Jasmine J. Clark	<b>Art Unit</b> 2815	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 11 is/are rejected.
- 7) ☒ Claim(s) 7-10 is/are objected to:
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 4/6/6 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                               | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                      | 5) <input type="checkbox"/> Notice of Informal Patent Application                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

***Claim Rejections - 35 USC § 102***

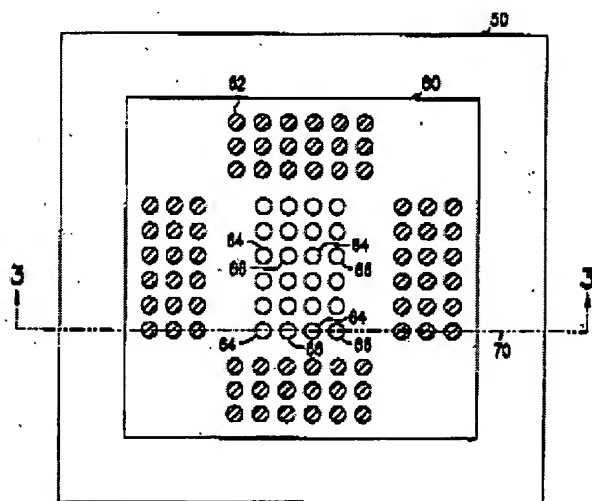
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-6, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakravorty et al. (US 2004/0238942 A1).

Chakravorty '942 discloses relating to an electronic device, comprising



**FIG. 2**

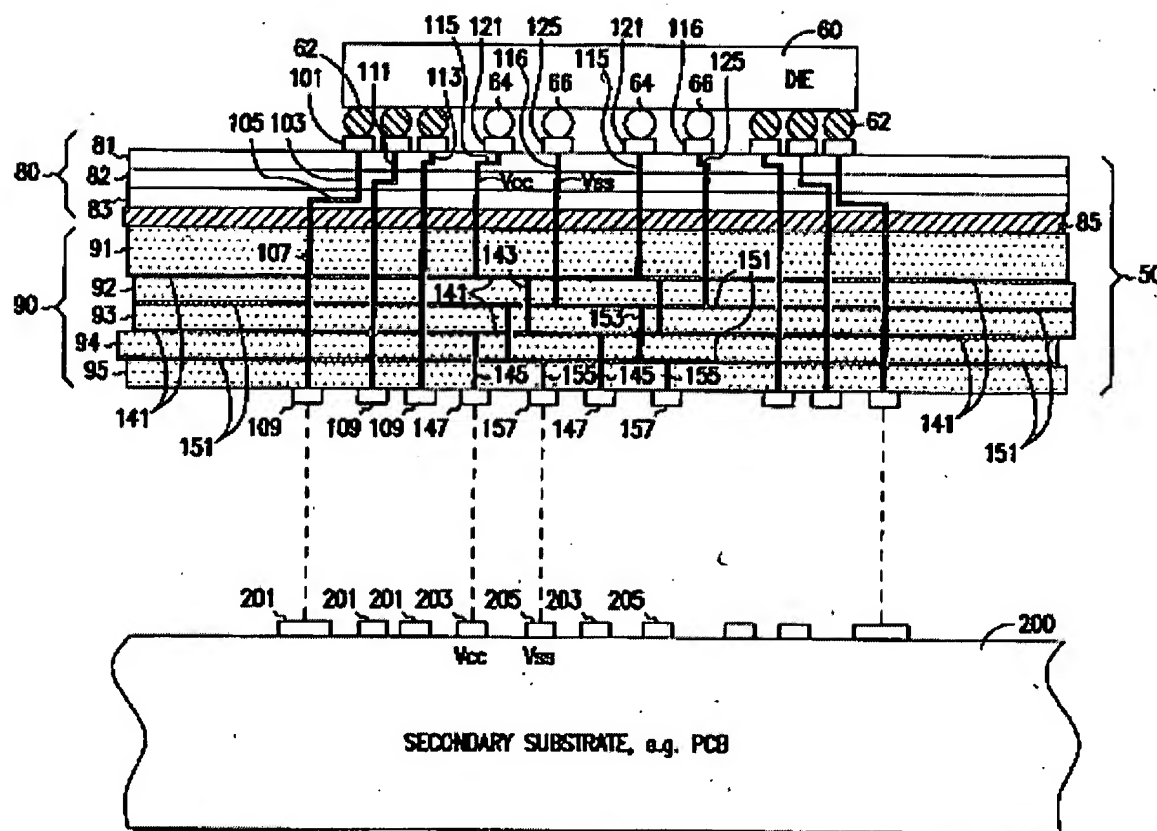


FIG. 3

a semiconductor device providing with a plurality of bond pads, of which bond pads a first portion is defined for ground connection and a second portion is defined for voltage supply (see paras [0028], [0029] and [0030]) and a third portion is defined for signal transmission (see para [0033]), and a carrier substrate (50) comprising a layer of dielectric material (see para [0020]) and having a first side and an opposed second side, the first side and the opposed second side are each provided with an electrically conductive layer, on which first side bond pads are present corresponding to the bond pads of the semiconductor device, and on which second side contact pads (109, ie.,) for external coupling are provided, the contact pads and the bond pads being subdivided into a first, a second and a third portion corresponding to the portions of the

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semiconductor device, the first and second portions of the bond pads being present laterally in an inner area (areas of solder balls 64 and 66 disposed) and the third portion (areas of solder balls 62 disposed) being present in an outer area around the inner area, wherein the semiconductor device is coupled to the carrier substrate in a flip-chip orientation, and the bond pads and the contact pads for voltage and ground connection ( $V_{cc}$  and  $V_{ss}$ ) are located correspondingly, so as to provide a direct path from the contact pads at the substrate to the corresponding bond pads of the semiconductor device, and the pads of the first and second portions (116, 121 and 125, for example) are arranged such that at least one direct dedicated to voltage supply connection acts as a coaxial center conductor.

Concerning claim 3 and 4, wherein the pads for ground and supply connections are arranged according to a chessboard pattern (see Fig. 2 above), and wherein a layer of dielectric material (81 and/or 95, i.e.,) (see paras [0033] and [0036]) extends from the first to the second side in the substrate.

Concerning claims 5 and 6, an electronic device as claimed in claim 1, characterized in that the bond pads of the third portion and the corresponding contact pads (through 109, i.e.,) for external coupling are interconnected through; interconnects defined in the conductive layer on the first side of the carrier substrate (50), and vertical interconnects through the carrier substrate (50) which, in the case of perpendicular projection on the conductive layer on the second side, have a substantial overlap with the contact pads for signal transmission (at least at an internal region of the third portion, see Fig. 3 above). Furthermore, an electronic device as claimed in claim 5,

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characterized in that a ground plane ( $V_{cc}$  and  $V_{ss}$ ) is defined in the conductive layer on the second side (i.e., 147 and 157) of the carrier substrate (50), and the mutual distance between the interconnects and the dielectric thickness of the carrier substrate are chosen such that the interconnects have transmission line characteristics. For the reason that the limitations of claim 10 are similar to claim 1, please see the above discussion.

### ***Allowable Subject Matter***

2. Claims 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The applied reference fails to disclose and/or suggest the followings:

- comprising a mechanical stiffener layer on the first side of the carrier substrate;
- comprising a heat dissipation layer on the first carrier substrate; and
- having a second semiconductor device that is provided with a direct path for ground voltage supply connection from its bond pads to the second side of the carrier substrate, on which second side contact pads for ground and voltage supply connection are present.

### ***References Cited***

3. The references are cited and should be carefully considered: Yeo et al. (US 6,608,379), Sathe (US 6,800,947), Yandentop et al. (US 6,717,066), Figueroa et al. (US

6,388,207 B1), and Jacobs (US 2003/0038378) discloses relating to an electronic device, comprising a semiconductor device provided with a plurality of bond pads including signal, power and ground connections, wherein the semiconductor device is coupled to the carrier substrate in a flip chip orientation. Sylvester (US 5,900,312) discloses an IC package including a mechanical stiffener layer disposed on a first side of a carrier substrate. Furthermore, a reference of Coenen (US 7,253,516) has been reviewed.

#### ***Telephone Inquiry Contacts***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine J. Clark whose telephone number is (571) 272-1726. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jjbc/2/1/8

**JASMINE CLARK**  
**PRIMARY EXAMINER**

A handwritten signature in black ink, appearing to read 'Jasmine Clark', written in a cursive style.